IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Xiaodong Jin et al.	Art Unit	: 2836
Serial No.	: 10/811,031	Examiner	: Scott Allen Bauer
Filed	: March 26, 2004	Conf. No.	: 1354
Title	: METHOD AND APPARATUS FOR IMPROVING SUPPLY NOISE REJECTION		

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BRIEF ON APPEAL

This Appeal Brief is submitted pursuant to the Notice of Appeal filed in the U.S. Patent and Trademark Office on December 18, 2007, and from the Notice of Panel Decision from Pre-Appeal Brief Review mailed on January 28, 2008.

(1) Real Party in Interest

The real party in interest is the assignee, Marvell International Ltd.

(2) Related Appeals and Interferences

There are no related appeals or interferences.

(3) Status of Claims

Claims 1-3, 5-11, 13-19, 21-26, 28-32, and 34-36 are pending and stand rejected. Claims 1, 9, 17, 24, and 31 are independent. Applicants traverse and appeal the rejection of these claims.

(4) Status of Amendments

The claims have not been amended subsequent to final rejection, and there are no unentered amendments.

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(5) Summary of Claimed Subject Matter

Claim 1

Claim Language	Support in Specification and/or FIGS.
A low noise amplifier, comprising:	*See, e.g.*, FIG. 5, no. 500; paras. [0015], [0041].
a radio frequency input; and	*See, e.g.*, FIG. 2, no. 20; FIG. 5, no. 502; paras. [0015], [0041].
an electrostatic discharge protection circuit including,	*See, e.g.*, FIGS. 2, 3, 6, 7, no. 206; paras. [0002]-[0003], [0010], [0015], [0029], [0035].
a pair of diodes each having a first and a second terminal;	*See, e.g.*, FIGS. 3, 6, nos. 300, 302; paras. [0011], [0035].
a first diode of the pair having a first terminal coupled to the radio frequency input and a second terminal directly coupled to a first supply;	*See, e.g.*, FIGS 3, 6, no. 300; paras. [0015], [0035].
a second diode of the pair having a second terminal coupled to the radio frequency input and a first terminal directly coupled to the first supply; and	*See, e.g.*, FIGS. 3, 6, no. 302; paras. [0015], [0035].
a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;	*See, e.g.*, FIGS. 2, 3, 6-9, no. 208; paras. [0003], [0011], [0031], [0032].

the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events away from the radio frequency input and through the first supply.	*See, e.g.*, FIGS. 2, 3, 6; paras. [0002], [0005]-[0008], [0015], [0029], [0031]-[0034], [0036]-[0039], [0045].

Claim 9

Claim Language	Support in Specification and/or FIGS.
A low noise amplifier, comprising:	*See, e.g.*, FIG. 5, no. 500; paras. [0015], [0041].
receiving means for receiving an RF input; and	*See, e.g.*, FIG. 2, no. 20; FIG. 5, no. 502; paras. [0015], [0041].
shunting means including,	*See, e.g.*, FIGS. 2, 3, 6, 7, no. 206; paras. [0002]-[0003], [0010], [0015], [0029], [0035].
a pair of diode means each having a first terminal and a second terminal;	*See, e.g.*, FIGS. 3, 6, nos. 300, 302; paras. [0011], [0035].
a first diode means of the pair having a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply;	*See, e.g.*, FIGS 3, 6, no. 300; paras. [0015], [0035].
a second diode means of the pair having a second terminal coupled to the receiving means and a first terminal	*See, e.g.*, FIGS. 3, 6, no. 302; paras. [0015], [0035].

directly coupled to the first supply; and	
a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;	*See, e.g.*, FIGS. 2, 3, 6-9, no. 208; paras. [0003], [0011], [0031], [0032].
the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events away from the receiving means and through the first supply.	*See, e.g.*, FIGS. 2, 3, 6; paras. [0002], [0005]-[0008], [0015], [0029], [0031]-[0034], [0036]-[0039], [0045].

Claim 17

Claim Language	Support in Specification and/or FIGS.
An electrostatic discharge protection circuit, comprising:	*See, e.g.*, FIGS. 2, 3, 6, 7, no. 206; paras. [0002]-[0003], [0010], [0015], [0029], [0035].
a pair of diodes each having a first terminal and a second terminal;	*See, e.g.*, FIGS. 3, 6, nos. 300, 302; paras. [0011], [0035].
a first diode of the pair having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply;	*See, e.g.*, FIGS 3, 6, no. 300; paras. [0015], [0035].
a second diode of the pair having a	*See, e.g.*, FIGS. 3, 6, no. 302; paras. [0015],

second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and	[0035].
a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;	*See, e.g.*, FIGS. 2, 3, 6-9, no. 208; paras. [0003], [0011], [0031], [0032].
the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events.	*See, e.g.*, FIGS. 2, 3, 6; paras. [0002], [0005]-[0008], [0015], [0029], [0031]-[0034], [0036]-[0039], [0045].

Claim 24

Claim Language	Support in Specification and/or FIGS.
An electrostatic discharge protection circuit for discharging electrostatic discharge events, comprising:	*See, e.g.*, FIGS. 2, 3, 6, 7, no. 206; paras. [0002]-[0003], [0010], [0015], [0029], [0035].
shunting means including,	*See, e.g.*, FIGS. 2, 3, 6, 7, no. 206; paras. [0002]-[0003], [0010], [0015], [0029], [0035].
a pair of diode means having a first terminal and a second terminal;	*See, e.g.*, FIGS. 3, 6, nos. 300, 302; paras. [0011], [0035].
a first diode means of the pair	*See, e.g.*, FIGS 3, 6, no. 300; paras. [0015],

having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply;	[0035].
a second diode means of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and	*See, e.g.*, FIGS. 3, 6, no. 302; paras. [0015], [0035].
a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;	*See, e.g.*, FIGS. 2, 3, 6-9, no. 208; paras. [0003], [0011], [0031], [0032].
the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events.	*See, e.g.*, FIGS. 2, 3, 6; paras. [0002], [0005]-[0008], [0015], [0029], [0031]-[0034], [0036]-[0039], [0045].

Claim 31

Claim Language	Support in Specification and/or FIGS.
A method for discharging electrostatic discharge, comprising:	*See, e.g.*, FIG. 4, no. 400; paras. [0012], [0040].
providing a first direct discharge path between an input/output pad and a first supply;	*See, e.g.*, Figs. 3, 6, no. 300; paras. [0012], [0014], [0015], [0035], [0040].

providing a second direct discharge path between the input/output pad and the first supply;	*See, e.g.*, Figs 3, 6, no. 302; paras. [0012], [0015], [0035].
a second diode of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and	*See, e.g.*, FIGS. 3, 6, no. 302; paras. [0015], [0035].
shunting electrostatic discharge current during positive and negative electrostatic discharge events through one of the first discharge path and the second discharge path	*See, e.g.*, FIG. 4, Nos. 404-414; paras. [0002], [0005]-[0008], [0011]-[0012]; [0015], [0029], [0031]-[0034], [0036]-[0039], [0040], [0045].

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 1-3, 5, 8-11, 13 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,738,248, ("Jenkins") in view of U.S. Patent No. 5,994,760, ("Duclos") and International Publication No. WO 02/05380 ("Rutfors").

Claims 17-19, 21, 24-26, 28, 31, 32 and 34 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Jenkins in view of Duclos.

(7) Argument

I. Rejections under 35 U.S.C. § 103(a)

The Examiner rejected claims 1-3, 5, 8-11, 13 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Jenkins in view of Duclos. The Examiner also rejected claims 17-19, 21, 24-26, 28, 31, 32 and 34 as allegedly being unpatentable over Jenkins in view of Duclos. Applicants respectfully traverse these rejections.

A. Claim 1 and its dependent claims

Claim 1 is directed to a low noise amplifier that includes a radio frequency input and an electrostatic discharge ("ESD") protection circuit to shunt ESD current during positive and negative ESD events away from the radio frequency input and through a first supply. The ESD protection circuit includes a pair of diodes and a separate ESD clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode of the pair has a first terminal coupled to the radio frequency input and a second terminal directly coupled to a first supply. The second diode of the pair has a second terminal coupled to the radio frequency input and a first terminal directly coupled to the first supply.

1. **The cited portion of art fails to teach or suggest a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply because there is no reasonable rationale for combining Duclos with Jenkins.**

The Examiner acknowledges that Jenkins' protection circuit 108 does not have Applicants' claimed separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event. The Examiner contends that Fig. 2 of Duclos shows Applicants' claimed ESD clamp and that it would have been obvious to incorporate Duclos' clamp "between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply." Applicants respectfully disagree. Applicants respectfully submit that the Examiner has not shown a reasonable rationale for combining Jenkins and Duclos.

Jenkins shows a protection circuit 108 that protects a differential input buffer 102 during ESD events. (Col. 3, lines 6-10). Jenkins discloses three embodiments of the protection circuit employing three different techniques for discharging ESD current to the positive and negative voltage supplies. Jenkins' first embodiment includes two back-to-back diode pairs coupled between the buffer inputs and a negative voltage supply (VSS). These diode pairs discharge ESD current directly to VSS. (Fig. 1; Col. 3, lines 16-20, 43-53). In Jenkins' second embodiment, the diode pairs are coupled between the buffer inputs and a positive voltage supply

(VDD) and discharge the ESD current to VDD. (Fig. 2; col. 4, lines 6-11). In Jenkins' third embodiment, a single diode pair is coupled between the buffer inputs and an intermediate node 304. (Fig. 3; Col. 4, lines 35-39). Jenkins' diodes D5 and D6 discharge current from over-voltages at the input to VDD and VSS, respectively, and form a voltage clamp that maintains the voltage between VSS and VDD at 1.4V. (Col. 4, lines 39-45).

The Examiner states that it would have been obvious to incorporate Duclos' voltage clamp between Jenkins' VDD and VSS terminals to provide "bidirectional protection to the buffer (102) from ESD occurring from the power supply." Applicants respectfully assert that Jenkins already discloses a voltage clamp between the VDD and VSS terminals for providing bidirectional ESD protection to the buffer. As shown in Jenkins' Fig. 3, diodes D5 and D6 form a voltage clamp between supplies VDD and VSS to protect the buffer 102 from ESD events occurring at either supply. (Fig. 3; col. 4, lines 39-45). No reasonable rationale exists to modify Jenkins' protection circuit to include Duclos' clamp – to the contrary, Jenkins teaches away from adding Duclos' clamp, because this addition would duplicate Jenkins' existing protection techniques.

The Examiner responds to Applicants' points by stating that "[a]lthough Jenkins provides a method of shunting ESD events between VDD and VSS in Fig. 3, this embodiment is not the only way to provide rail-to-rail protection to the circuit. In fact, if one of ordinary skill in the art where [sic] concerned with providing bi-directional protection between VDD and VSS, the embodiment of Jenkins' Fig. 3 would not be used." As the Examiner himself acknowledges, Jenkins already discloses a method of providing rail-to-rail protection. In fact, Jenkins discloses *three different* protection circuit configurations, one of which – shown in Fig. 1 – follows the same back-to-back diode clamp configuration taught by Duclos.

Given that Jenkins already discloses a clamp protection circuit, one of skill in the art would not have seen any reason to combine the elements of Duclos and Jenkins in the manner suggested by the Examiner. *See KSR Intl. Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007) ("[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does"). Rather, the Examiner's asserted combination is premised on the improper use of hindsight. *See, e.g., Orthopedic Equipment Co., Inc. v. U.S.*, 702 F.2d 1005, 1012 (Fed. Cir. 1983) ("It is wrong to

use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit."). Applicants respectfully assert that the Examiner has not presented a reasonable rationale for combining Jenkins and Duclos.

For at least these reasons, Applicants respectfully assert that the Examiner has not carried his burden of establishing a *prima facie* case of obviousness with respect to the Jenkins and Duclos references. Therefore, claim 1 and all claims depending from claim 1 are allowable.

2. The cited portion of art fails to teach or suggest a radio frequency input because there is no reasonable rationale for combining Rutfors and Jenkins.

The Examiner also acknowledges that Jenkins fails to teach that the input is a radio frequency input. Instead, the Examiner contends that Rutfors shows this limitation and that it would have obvious to combine the teachings of Jenkins and Rutfors "for the purpose of providing ESD protection to a wireless circuit thus preventing the [low noise amplifier] from being damaged." Applicants respectfully disagree.

Again, Applicants submit that the Examiner has not carried his burden of establishing a *prima facie* case of obviousness with respect to the asserted combination of Jenkins and Rutfors. The Examiner states that "the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art apparatus satisfying the claimed structural limitations." This point is irrelevant, however, to the Examiner's burden of articulating a reason to combine the asserted references. It is insufficient for the Examiner to merely state the advantages of a particular limitation, i.e., to merely note that adding ESD protection would be desirable to prevent damage to an amplifier. The fact that references *can* be combined is insufficient to establish obviousness – rather, the Examiner must point to a reason for this modification to be made. *See KSR Intl. Co.*, 127 S.Ct. at 1741; *see also In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991) ("It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. . . The references themselves must provide some teaching whereby the applicant's combination would have been obvious."). The

Examiner has cited to no such suggestion in Rutfors or in the art and has therefore failed to satisfy his burden with respect to obviousness.

For at least these additional reasons, Applicants respectfully assert that the Examiner has not carried his burden of establishing a *prima facie* case of obviousness with respect to the Rutfors and Jenkins references. Therefore, claim 1 and all claims depending from claim 1 are allowable.

3. The cited portion of art fails to teach or suggest that the low voltage supply floats during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

Claim 6 is also separately allowable for at least the following additional reasons. Claim 6 recites that the low voltage supply floats during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse. In rejecting claim 6, the Examiner states that "Jenkins et al. in view of Duclos and Rutfors et al., *in Figure 3*, discloses the low noise amplifier [of claim 6]" (emphasis added). Applicants responded previously to this rejection by pointing out that Jenkins' Fig. 3 shows that Jenkins' protection circuit will not operate correctly if VSS is allowed to float: diode D6 will not conduct, and the ESD current will be discharged directly into buffer 102.

The Examiner now asserts that "the circuit of [Jenkins'] Fig. 3 is not relied upon for the rejection... Rather, Fig. 1 of Jenkins in combination with Duclos would perform the limitations of Claims 6 and 7." However, Fig. 1 of Jenkins does not cure this deficiency because Fig. 1 does not include any path between the input and high voltage supply to permit a radio frequency input to high voltage supply positive discharge pulse or negative discharge pulse. In Jenkins' Fig. 1, two pairs of back-to-back diodes are coupled between the differential inputs and *VSS*, the *negative* supply. (Col. 2, lines 47-54; col. 3, 16-21). The Examiner's proposed modification of Jenkins to include Duclos' clamp does not supply this missing path because he asserts that Duclos' clamp would be incorporated "between the terminals of VDD and VSS" – not between the input and VDD.

Additionally, Jenkins' low voltage supply VDD does not merely float during ESD events, as recited by Applicants' claim. VDD and VSS serve to bias the buffer 102, and VSS must be

biased to a voltage that is less than VDD (generally, 0V). (Col. 2, lines 47-54). For at least these reasons, Applicants respectfully assert that claim 6 is separately allowable.

4. The cited portions of the art fail to teach or suggest that the high voltage supply floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

Claim 7 is also separately allowable for at least the following additional reasons. Claim 7 recites that the high voltage supply floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse. As discussed above, however, Jenkins uses positive supply VDD and negative supply VSS to bias the buffer 102. (Col. 2, lines 47-54). VDD must be biased to a voltage that is greater than VSS – generally, 1V – and does not float during ESD events. (Col. 2, lines 49-54). The Examiner's proposed modification of Jenkins to include Duclos' clamp does not cure this deficiency: it provides a maximum that the voltage differential may not exceed, but it does not preserve the biasing conditions for the buffer's proper operation.

For at least these reasons, Applicants respectfully assert that claim 7 is separately allowable.

B. Claim 9 and its dependent claims

Claim 9 is directed to a low noise amplifier that includes receiving means for receiving an RF input and shunting means to shunt ESD current during positive and negative ESD events away from the receiving means and through a first supply. The shunting means includes a pair of diode means and a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode means of the pair has a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply. The second diode means of the pair has a second terminal coupled to the receiving means and a first terminal directly coupled to the first supply.

As discussed above, the cited portions of the art fail to teach or suggest a separate clamping means directly coupled between a high voltage supply and a low voltage supply because the Examiner has not carried his burden of establishing a *prima facie* case of obviousness for the combination of Duclos and Jenkins. Additionally, the cited art fails to teach

or suggest receiving means for receiving an RF input because the Examiner has not carried his burden of establishing a *prima facie* case of obviousness for the combination of Rutfors and Jenkins. Therefore, claim 9 and all claims depending from claim 9 are allowable for at least the reasons given above with respect to claim 1.

Claim 14 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 15 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

C. Claim 17 and its dependent claims

Claim 17 is directed to an ESD protection circuit to shunt ESD current during positive and negative ESD events. The protection circuit includes a pair of diodes and a separate ESD clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode of the pair has a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply. The second diode of the pair has a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply.

As discussed above, the cited portions of the art fail to teach or suggest a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply because the Examiner has not carried his burden of establishing a *prima facie* case of obviousness for the combination of Duclos and Jenkins. Therefore, claim 17 and all claims depending from claim 17 are allowable for at least the reasons given above with respect to claim 1.

Claim 22 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 23 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

D. Claims 24 and its dependent claims

Claim 24 is directed to an ESD protection circuit that includes shunting means for shunting ESD current during positive and negative ESD events and a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a

discharge path there between during an ESD event. The shunting means includes a pair of diode means. The first diode means of the pair has a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply. The second diode means of the pair has a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply.

As discussed above, the cited portions of the art fail to teach or suggest a separate clamping means directly coupled between a high voltage supply and a low voltage supply because the Examiner has not carried his burden of establishing a *prima facie* case of obviousness for the combination of Duclos and Jenkins. Therefore, claim 24 and all claims depending from claim 24 are allowable for at least the reasons given above with respect to claim 1.

Claim 29 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 30 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

E. Claim 31 and its dependent claims

Claim 31 is directed to a method for discharging ESD that includes providing a first direct discharge path between an input/output pad and a first supply, providing a second direct discharge path between the input/output pad and the first supply, providing a third discharge path between the first supply and a second supply during an ESD event; and shunting ESD current during positive and negative ESD events through one of the first discharge path and the second discharge path.

The Examiner suggests that Jenkins' Fig. 3 shows Applicants' claimed steps of providing first and second direct paths between an input and a first supply, and shunting ESD current during positive and negative ESD events through one of the first discharge path and the second discharge path. The Examiner acknowledges that Jenkins does not teach providing a third discharge path between the first supply and a second supply during an electrostatic discharge event. The Examiner suggests that Duclos' ESD clamp in Fig. 2 meets this limitation. The Examiner further suggests that it would have been obvious to incorporate Duclos' ESD clamp

into Jenkins' design "for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply."

As discussed above with respect to claim 1, the Examiner has not carried his burden of establishing a *prima facie* case of obviousness. Jenkins already discloses a protection circuit for protecting the buffer from ESD events occurring at the supply, and this disclosed protection circuit uses a clamp configuration. Modifying Jenkins to include Duclos' clamp would be redundant in view of this existing protection. Applicants respectfully assert that claim 31 and all claims depending from claim 31 are allowable for at least these reasons.

Claim 35 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 36 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

Please charge the fee for filing a brief in the amount of $510 and any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Appendix of Claims

1. A low noise amplifier, comprising:

a radio frequency input; and

an electrostatic discharge protection circuit including,

a pair of diodes each having a first and a second terminal;

a first diode of the pair having a first terminal coupled to the radio frequency input and a second terminal directly coupled to a first supply;

a second diode of the pair having a second terminal coupled to the radio frequency input and a first terminal directly coupled to the first supply; and

a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;

the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events away from the radio frequency input and through the first supply.

2. The low noise amplifier of claim 1, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices.

3. The low noise amplifier of claim 1, wherein the first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply,

if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

5. The low noise amplifier of claim 3, wherein the positive and negative electrostatic discharge events include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

6. The low noise amplifier of claim 5, wherein the low voltage supply floats during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

7. The low noise amplifier of claim 5, wherein the high voltage supply floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

8. The low noise amplifier of claim 1, wherein the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

9. A low noise amplifier, comprising:

receiving means for receiving an RF input; and

shunting means including,

a pair of diode means each having a first terminal and a second terminal;

a first diode means of the pair having a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply;

a second diode means of the pair having a second terminal coupled to the receiving means and a first terminal directly coupled to the first supply; and

a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;

the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events away from the receiving means and through the first supply.

10. The low noise amplifier of claim 9, wherein the shunting means is formed by one of polymer device means and metal oxide silicon device means.

11. The low noise amplifier of claim 9, wherein the first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the shunting means is not directly coupled to a corresponding high voltage supply,

if the first supply means is a high voltage supply, then the shunting means is not directly coupled to a corresponding low voltage supply.

13. The low noise amplifier of claim 11, wherein the positive and negative electrostatic discharge events include a receiving means to high voltage supply positive discharge pulse, a receiving means to high voltage supply negative discharge pulse, a receiving means to low voltage supply positive discharge pulse, and a receiving means to low voltage supply negative discharge pulse.

14. The low noise amplifier of claim 13, wherein the low voltage supply floats during the receiving means to high voltage supply positive discharge pulse and the receiving means to high voltage supply negative discharge pulse.

15. The low noise amplifier of claim 13, wherein the high voltage supply floats during the receiving means to low voltage supply positive discharge pulse and the receiving means to low voltage supply negative discharge pulse.

16. The low noise amplifier of claim 9, wherein the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

17. An electrostatic discharge protection circuit, comprising:

a pair of diodes each having a first terminal and a second terminal;

a first diode of the pair having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply;

a second diode of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and

a separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;

the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events.

18. The circuit of claim 17, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices.

19. The circuit of claim 17, wherein first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply,

if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

21. The circuit of claim 19, wherein the positive and negative electrostatic discharge events include an input/output pad to high voltage supply positive discharge pulse, an input/output pad to high voltage supply negative discharge pulse, an input/output pad to low voltage supply positive discharge pulse, and an input/output pad to low voltage supply negative discharge pulse.

22. The circuit of claim 21, wherein the low voltage supply floats during the input/output pad to high voltage supply positive discharge pulse and the input/output pad to high voltage supply negative discharge pulse.

23. The circuit of claim 21, wherein the high voltage supply floats during the input/output pad to low voltage supply positive discharge pulse and the input/output pad to low voltage supply negative discharge pulse.

24. An electrostatic discharge protection circuit for discharging electrostatic discharge events, comprising:

shunting means including,

a pair of diode means having a first terminal and a second terminal;

a first diode means of the pair having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply;

a second diode means of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and

a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event;

the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events.

25. The electrostatic discharge protection circuit of claim 24, wherein the shunting means is formed by one of polymer device means and metal oxide silicon device means.

26. The electrostatic discharge protection circuit of claim 24, wherein the first supply is one of a low voltage supply and a high voltage supply, and

if the first supply is a low voltage supply, then the shunting means is not directly coupled to a corresponding high voltage supply,

if the first supply means is a high voltage supply, then the shunting means is not directly coupled to a corresponding low voltage supply.

28. The electrostatic discharge protection circuit of claim 26, wherein the positive and negative electrostatic discharge events include an input/output pad to high voltage supply positive discharge pulse, an input/output pad to high voltage supply negative discharge pulse, an input/output pad to low voltage supply positive discharge pulse, and an input/output pad to low voltage supply negative discharge pulse.

29. The electrostatic discharge protection circuit of claim 28, wherein the low voltage supply floats during the input/output pad to high voltage supply positive discharge pulse and the input/output pad to high voltage supply negative discharge pulse.

30. The electrostatic discharge protection circuit of claim 28, wherein the high voltage supply floats during the input/output pad to low voltage supply positive discharge pulse and the input/output pad to low voltage supply negative discharge pulse.

31. A method for discharging electrostatic discharge, comprising:

providing a first direct discharge path between an input/output pad and a first supply;

providing a second direct discharge path between the input/output pad and the first supply;

providing a third discharge path between the first supply and a second supply during an electrostatic discharge event; and

shunting electrostatic discharge current during positive and negative electrostatic discharge events through one of the first discharge path and the second discharge path.

32. The method of claim 31, wherein providing a first discharge path and a second discharge path includes providing a first discharge path and a second discharge path between the input/output pad and one of a low voltage supply and a high voltage supply,

if the first discharge path and the second discharge path are provided between the input/output pad and a low voltage supply, then not providing a direct discharge path between the input/output pad and a corresponding high voltage supply,

if the first discharge path and the second discharge path are provided between the input/output pad and a high voltage supply, then not providing a direct discharge path between the input/output pad and a corresponding low voltage supply.

34. The method of claim 32, wherein shunting electrostatic discharge current includes shunting one or more of an input/output pad to high voltage supply positive discharge pulse, an input/output pad to high voltage supply negative discharge pulse, an input/output pad to low voltage supply positive discharge pulse, and an input/output pad to low voltage supply negative discharge pulse.

35. The method of claim 34, wherein shunting an input/output pad to high voltage supply positive discharge pulse and shunting an input/output pad to high voltage supply negative discharge pulse includes floating the low voltage supply.

36. The method of claim 34, wherein shunting an input/output pad to low voltage supply positive discharge pulse and shunting an input/output pad to low voltage supply negative discharge pulse includes floating the high voltage supply.

Evidence Appendix

None.

Related Proceedings Appendix

None.